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(54) Title: CLUSTERED ILP PROCESSOR AND A METHOD FOR ACCESSING A BUS IN A CLUSTERED ILP PROCESSOR
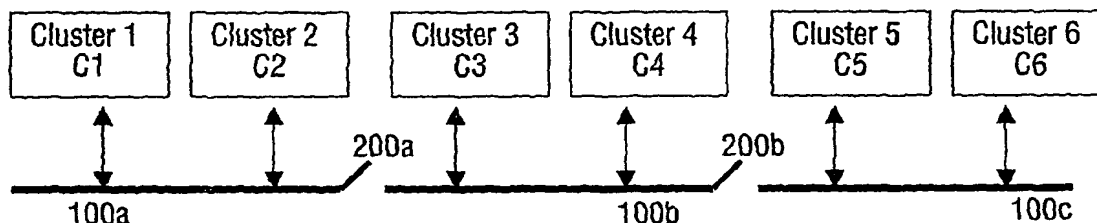
(57) Abstract: The basic idea of the invention is to add switches along a bus, in order divide the bus into smaller independent segments by opening/closing said switches. A clustered Instruction Level Parallelism processor comprises a plurality of clusters (C1 - C6) each comprising at least one register file (RF) and at least one functional unit (FU), a bus means (100) for connecting said clusters (C1 - C6), wherein said bus (100) comprises a plurality of bus segments (100a, 100b, 100c), and switching means (200), which is arranged between adjacent bus segments (100a, 100b, 100c). Said switching means (200) are used for connecting or disconnecting adjacent bus segments (100a, 100b, 100c). Furthermore, a method for accessing a bus (100) in a clustered Instruction Level Parallelism processor is shown. Said bus (100) comprises at least one switching means (200) along said bus (100). A cluster can either perform a sending operation based on a source register and transfer word or a receiving operation based on a designation source register and a transfer word. Said switching means are then opened/closed according to said transfer word.